

Radiation Testing and Evaluation Issues for Modern Integrated Circuits

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Abstract. Changes in modern integrated circuit (IC) technologies have modified the way we approach and conduct radiation tolerance and testing of electronics. These changes include scaling of geometries, new materials, new packaging technologies, and overall speed and device complexity challenges. In this short course section, we will identify and discuss these issues as they impact radiation testing, modeling, and effects mitigation of modern integrated circuits. The focus will be on CMOS-based technologies, however, other high performance technologies will be discussed where appropriate. The effects of concern will be: Single Event Effects (SEE) and steady state total ionizing dose (TID) IC response. However, due to the growing use of optoelectronics in space systems issues concerning displacement damage testing will also be considered. This short course section is not intended to provide detailed “how-to-test” information, but simply provide a snapshot of current challenges and some of the approaches being considered.

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1 Introduction

The objective of this course is to identify and discuss the issues involved with radiation testing and characterization of silicon based, deep submicron, integrated circuits and system-on-chip devices. The focus will be on Single Event Effects (SEE) with some mention of steady state total ionizing dose (TID) testing and characterization. However, due to the growing use of optoelectronics in these complex circuits displacement damage testing and characterization will also be discussed. The impact of changes in technology and circuit design issues such as circuit design complexity, operating speed, construction (e.g. number of layers of metal), packaging, circuit technology mix (e.g. digital, analog/mixed-signal, volatile and non-volatile

memory, etc) and other salient features impact testing and characterization will be identified and discussed.

Finally, recommendations to help address these issues will be provided and discussed.

2 Assumptions

It is assumed that the readers of this short course have a working familiarity with basic solid state electronics technology, space radiation effects on electronics as well as the basics of radiation testing. We refer the reader to the NASA RadHome website for further background material [radhome].

The technology covered herein is mainstream CMOS technology with only limited mention of advanced mixed signal, etc. A complete discussion of all semiconductor technologies is outside the scope of this document.

3 Advanced Integrated Circuit Characteristics

3.1 IC Technology Advances:

The most profound effect on SEE performance concerning future semiconductor manufacturing trends is that of feature size scaling. Scaling is too often thought of as only reducing the geometric feature size of a transistor down to 90nm and below, but is much more complex than that in reality [see Figure 1a-b International Technology Roadmap for Semiconductors (ITRS) Roadmap] [ITRS01]. Technology changes may also include in new materials (e.g., alternative-K dielectrics), oxide changes, material resistance, newer materials (e.g., SiGe), changes in interconnect structures, etc. [Figure 1c]. This results in changes to device circuitry that manifest themselves as lower operating voltages, lower nodal capacitance and higher integration density, all of which serve to increase Single Event Upset (SEU) and Single Event Transient (SET) sensitivity and the potential for Multiple-bit Upset (MBU) effects. In general, one can discuss the impact of these changes to radiation test and characterization as geometric or operational implications. The following sections of this document are a snapshot of radiation issues related to these scaled technologies.

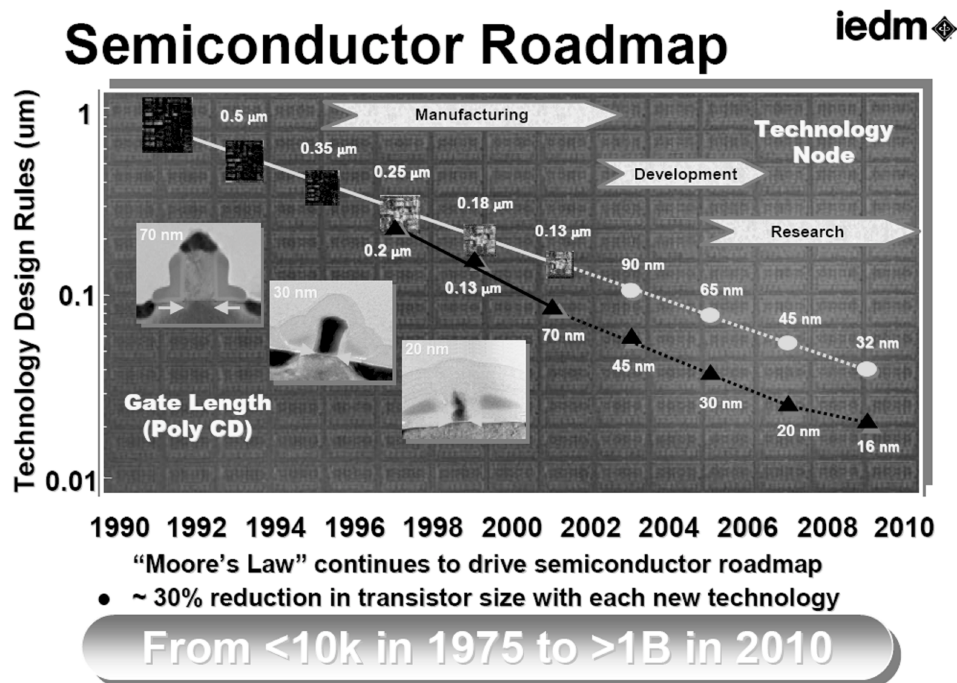
**Figure 1a ITRS Roadmap
Future Technology Trends**

Feature	2001	2003	2005	2007	2010	2016
Technology Node (μm)	130	100	70	65	45	22
Microprocessor <u>Printed</u> Gate Length (μm)	90	65	45	35	33	22
Microprocessor <u>Physical</u> Gate Length (μm)	65	45	32	25	18	9
Gate thickness (Equivalent oxide thickness nm)	1.3-1.6	1.1-1.6	0.8-1.3	0.6-1.1	0.5-0.8	0.4-0.5
Transistor per IC (M Transistors)	97	153	243	386	773	3,093
Wafer Size (mm)	300	300	300	300	300	450
On Chip Frequency (MHz)	1,684	3,088	5,173	6,739	11,511	28,751
Number of Metal Levels	7	8	8-9	9	9-10	10
Minimum Number of Masks	24	24	26	28	28	30
Power Supply (V)	1.2	1.0	0.9	0.7	0.6	0.4
Power Dissipation (W)	130	150	170	190	218	288
Cost per Transistor (microcents/transistor)	97	49	24	12	4.3	0.5

Source: 2001 International Technology Roadmap for Semiconductors. Values are for high performance microprocessors. [ITRS01].

The values given are for high performance logic devices like microprocessors. Some of the values presented are different for low-cost, for battery-operated logic, for Dynamic Random Access Memories (DRAM) and for Application Specific Integrated Circuits (ASIC) applications.

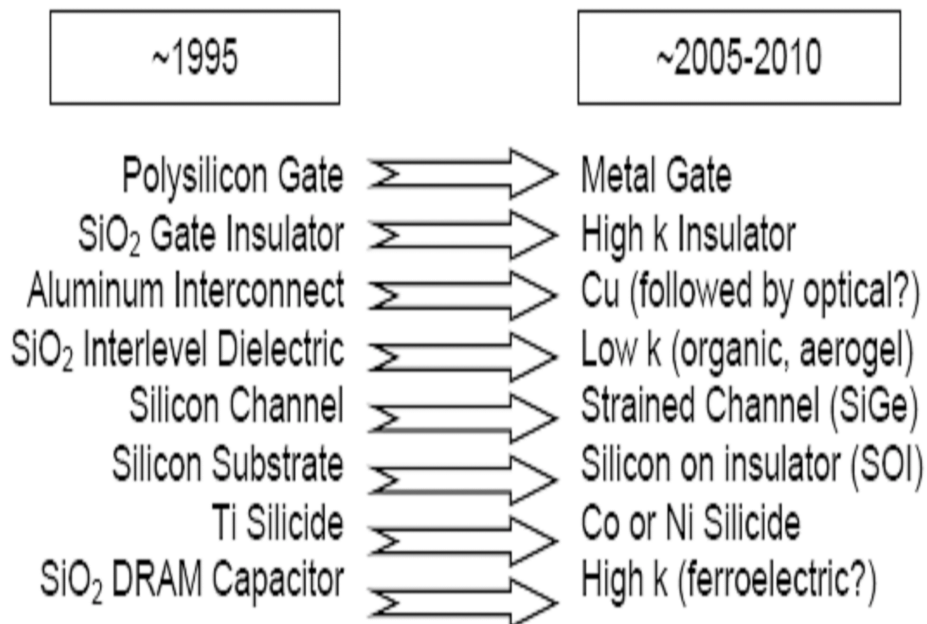
Figure 1b: ITRS Roadmap – CMOS Scaling



[ITRS01]

Figure 1c: IC Technology Trends

Virtually all of the Materials used to fabricate IC’s in 1995 will be different in 2010
A&T Dellin, 2005, 21st Century Semiconductor Technology

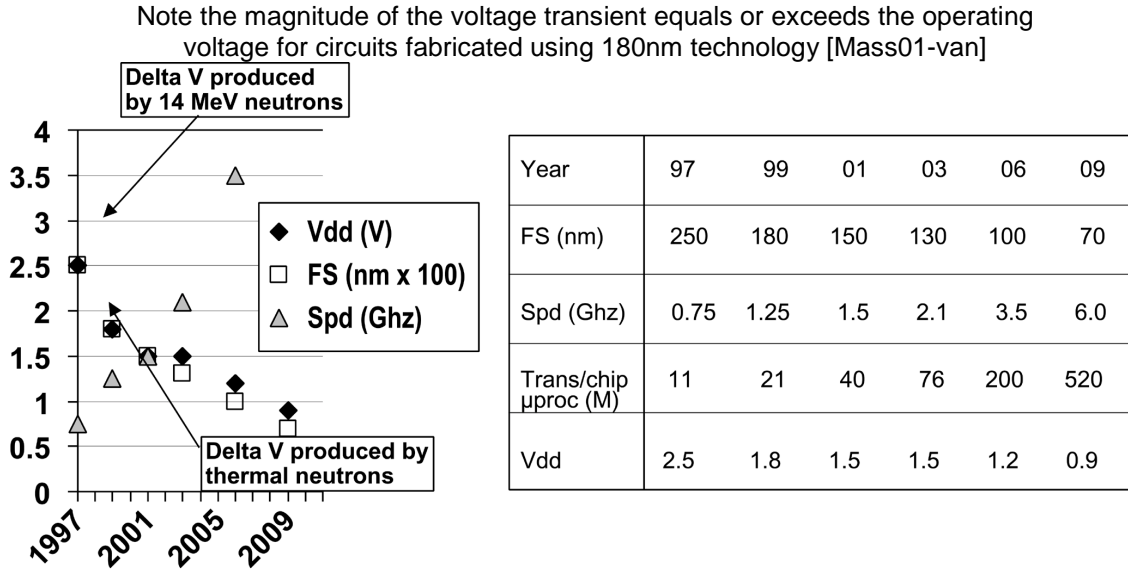


[Dell05]

Another way to look at the effect of scaling concerning SEE is to realize that the charge deposited by an energetic particle or heavy ion is invariant and the voltage transient produced proportional to deposited charge. Thus, as we reduce the critical charge required to produce an

upset (through operating voltage and nodal capacitance reductions) the sensitivity of a specific circuit can only increase. As an example, Figure 2 compares the magnitude of various voltage transients to operating voltage as a function of feature size [Mass01-van].

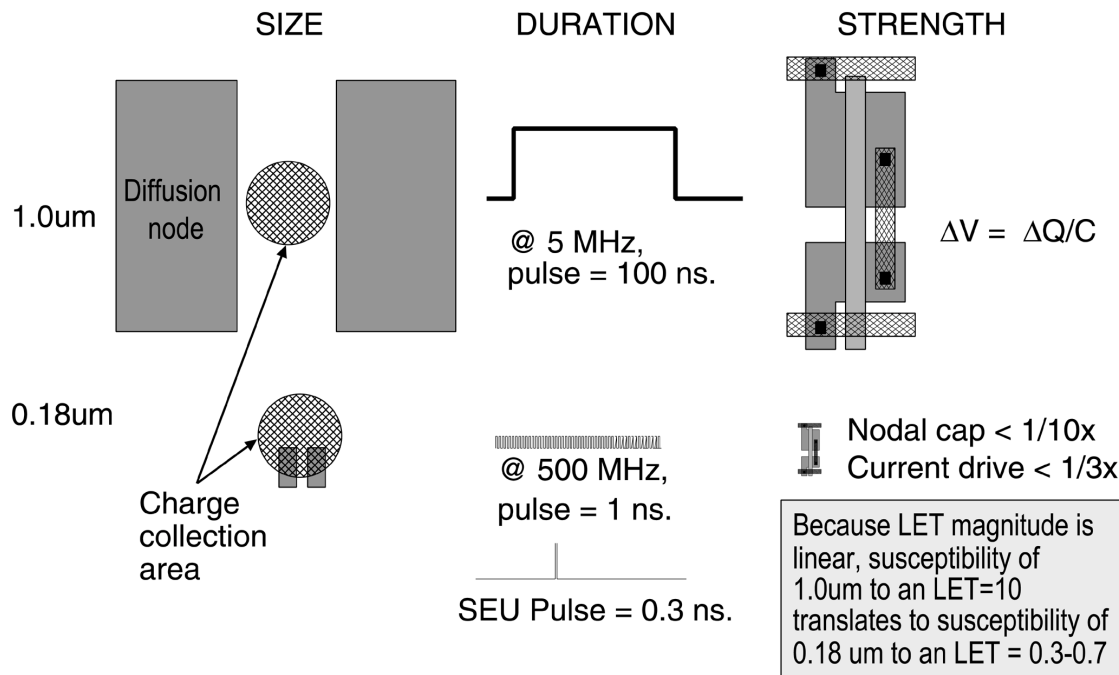
Figure 2: Operating Voltage versus Voltage Transient Magnitude for 1MeV and 14 MeV neutrons



Another characteristic of advanced microelectronics has to do with the trend to operate at increasingly higher clock speeds and the impact of this on SET performance. The capability to operate at these higher speeds has a twofold impact in that (1) the lower propagation delay of an individual inverter stage (or higher bandwidth) allows the voltage transients caused by particle strikes to propagate further through a multi-stage circuit without attenuation and (2) the higher clock rates provide more opportunity for a transient to be latched into a storage element (DFF or equivalent). Thus, one could postulate that there will be a cross-over point where SET induced error rates will exceed the traditional SEU error-rates as predicted by Dodd, Mavis and Benedetto, et-al. [Bene04].

Additionally, as we increase circuit density, we reach a situation where the radius of a strike now encompasses an entire memory cell or multiple transistors in the cell. This further exacerbates SEE sensitivity as shown in Figure 3. This issue is further complicated when we place these cell or circuit elements in closer proximity to each other, thus further increasing the probability of a multiple node strike within a circuit such as a latch. Note that even the operation of a hardened latch can be compromised if multiple nodes are simultaneously struck by a single energetic particle. This will be discussed in further detail in Section 6.

Figure 3: Comparison of the Impact of a Heavy Ion Strike for 1.0-micron and 0.18-micron Technologies, [Hadd05]



Beyond the direct ionization approach described above (charge being deposited), the ions (whether heavy ions or protons) also interact with the semiconductor through nuclear interactions causing secondary particles to be created. These secondary particles can then deposit sufficient energy to cause upsets to occur. If the sensitivity to these secondary particles scales as one would expect, device error rates will increase as well. This would require new means of predicting rates versus the industry standard CREME96 tool. The effect of these secondary particles is further exacerbated by the increasing use of high Z materials above the semiconductors active regions that contribute to the production of these particles.

Other trends that bode ill for SEE sensitivity include, but are not limited to:

- A trend away from the use of epitaxial-layered substrates, and
- Memory devices and microprocessors with multi-threading capability further increasing issues with Single Event Functional Interrupt (SEFI) and SEFI mitigation. [Irom04]

Considering the holding voltage of ~1.2V, Single Event Latchup (SEL) may cease to be a concern when operating voltages reach the < 1 volt range. However, until then, this failure mode must continue to be evaluated. Several trends will affect SEL sensitivity. These include:

- The trend to the elimination of epitaxial wafers for bulk designs which can further exacerbate this failure mode,
- The increasing use of Silicon on Insulator (SOI) wafers which will serve to eliminate SEL, and,
- Asymmetry of device layouts which will do what?

In a recent paper provided at the IEEE International Reliability Physics Symposium (IRPS) [Bose05], a comprehensive study of electrically induced latchup was conducted for four generations of IC's (180, 130, 90 and 65 nm CMOS technologies) and concluded that scaling trends have resulted in reduction of intrinsic process sensitivity to latchup, however the performance boosts resulting from scaling are promoting the potential for enhanced latchup stimuli. Circuit performance factors such as faster signal transitions and higher slew-rates

promote higher displacement currents that can enhance SEL sensitivity. Also, new complex testing requirements have been reported to have induced latchup failures [Chat04]. Additionally, it has been noted that the smaller distances between pads can also engender latchup [Salc03]. Finally, neutron induced latchup has been seen in SRAM's at ground level [Dodd04- IRPS].

3.2 Circuit-level Advances

Other considerations affecting the utilization, testing and characterization of advanced IC's related to the increased functionality and design complexity associated with these devices to include the following attributes:

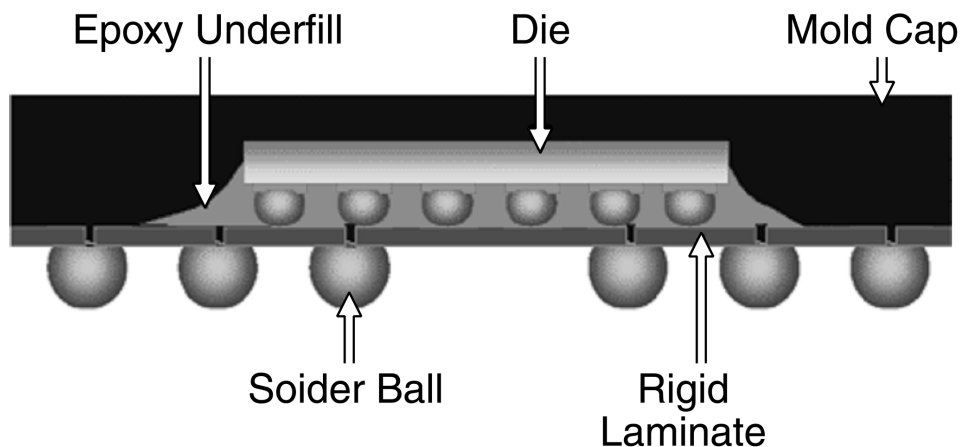
- **Intelligence:** Circuits contain embedded microprocessors, microcontrollers, programmable fabric and other circuits that allow some degree of autonomous operation and a variety of operating configurations that must be evaluated. This attribute also makes the identification and selection of an appropriate set of test vectors and fault coverage difficult. Also, many of these devices have built in fault protection (e.g., Error Detection and Correction (EDAC), voting schemes, etc.) that can affect testing and error-rate prediction.
- **Flexibility or programmability:** Circuits are being constructed with embedded Static Random Access Memory (SRAM) or Electrically Erasable Programmable Read-Only Memory (EEPROM) based programming capability that can be upset such that the architecture configuration of a circuit is lost or rearranged. This attribute can affect the approach to testing and characterization for both SEU and TID depending on the storage mechanism
- **Complexity:** Circuits are comprised of a variety of different circuit types and possibly technologies with different failure modes and sensitivities that include, but are not limited too, CMOS digital logic and volatile memory; floating gate or some other type of non-volatile memory (e.g., EEPROM, Ferro-Electric Random Access Memory (FERAM or FRAM), Chalcogenide Random Access Memory (C-RAM), etc.); CMOS analog/mixed-signal circuits (e.g., Analog to Digital Converters (ADC), Digital to Analog Converters (DAC), Serializer/Deserializer (SERDES), Low Voltage Differential Signaling (LVDS), voltage references, etc.), optoelectronic couplers and others. This complexity impacts error-rate predictions due to the various sensitive cross-sections and linear energy transfers (LETs) that are involved with an IC, test performance, test facility and test beam selection and a variety of other specific testing considerations.
- **Integration density:** Circuits are comprised of literally millions of critical nodes making fault coverage and test vector selection difficult. Also, the issue of MBU concerning error-rate predictions is affected by this factor.
- **Hidden Circuit Features:** Circuits often have many thousands of registers, built-in test elements, and other embedded circuits that are not identified by the manufacturer but can influence the radiation response of the overall device. These areas of the device may not be accessible to the external user.
- **Multi-layered construction:** Circuits are often fabricated using many levels of metal and complex packaging that make the interrogation of critical nodes using most SEE test facilities difficult if not impossible due to beam energy limitations. These construction methods also preclude the use of diagnostic tools such as lasers or ion-micro beams. In addition, concerning SEE testing, the over-layers can contribute secondary particles that influence the radiation response and make error-rate prediction difficult. Finally, these metal layers and other construction methods such as the use of high Z metals can cause dose-enhancement effects that are difficult to predict but have the potential to impact circuit lifetimes in a steady state TID radiation environment.

- **Power Requirements:** Circuits run “hot,” consuming significant amounts of power. Testing in a vacuum chamber or other restricted space must consider this issue.
- **Speed of operation:** The high operating speeds of these circuits require that SEE testing at or near the intended operating speed of the device be accomplished to obtain conservative error-rate estimates. For typical SEE test set-ups that require relatively long cabling, this requirement poses a significant problem.

3.3 Packaged Component Trends

These are several factors concerning packaging that have further complicated our ability to perform SEE testing and characterization. The most salient of these includes; (1) the use of plastic encapsulation and (2) the transition from relatively simple ceramic in-line packages to complex methods such as flip-chip ball grid array (FC BGA) packages such as the one shown in Figure 4. Plastic encapsulation has significantly complicated device SEE test preparation since removal without damaging the device under test (DUT) can be a time consuming and difficult endeavor. [Swift05]. The issues associated with the use of FC BGA package technology, however, are more profound due to inherent SEE test facility beam energy limitation. Although there are a few exceptions, the primary SEE facilities cannot provide sufficiently energetic beams to penetrate these complex packages and thus, significant effort is required to prepare the Device Under Test (DUT) via substrate thinning, package modification or complete re-packaging.

Figure 4: FC BGA



In subsequent sections of this course, the impact of the above noted attributes will be discussed with respect to their effect on device radiation response characterization and the adequacy of the test and characterization infrastructure to meet the demands imposed by them.

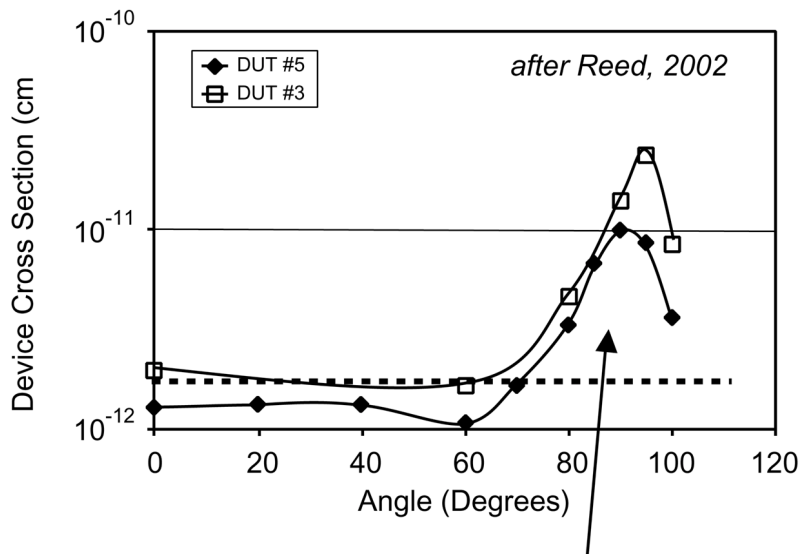
4 Representative Radiation Test and Modeling Issues Engendered by Advances in IC Technology

In this section, we will examine the impact of the characteristics and attributes of these advanced microelectronic devices concerning radiation testing, modeling and simulation.

These impacts or issues can be grouped into several categories that include:

- **Device physics:** In this category, issues such as 3-D charge collection and generation modeling and simulation in highly scaled devices, the impact of secondary generation on soft error rate (SER), limitations on sensitive volume assumptions, angular strike response and other issues associated with the present state-of-the-art understanding of the basic mechanisms associated with ionizing radiation effects in ultra-deep-submicron semiconductor electronics. Examples of issues that highlight shortfalls in the present knowledge base are shown in Figures 5 (showing unanticipated directionality effects from proton interactions in SOI technologies) [Reed02] and 6 (showing anomalous charge collection in SiGe devices) [Mars04] where discrepancies between anticipated and actual test results are depicted.
- **Radiation testing issues including test implementation and test facility limitations:** At present, the traditional methods concerning implementing SEE testing impose severe limitations with respect to obtaining a conservative characterization of the radiation response of advanced IC's. Simply stated, the need to test at realistic clock speeds, commensurate with actual IC operation, is not possible using the traditional approach that relies on bringing signals in and out of the DUT through long cables. Signal, thermal, power, device and cable input/output (I/O), and data capture are among the more intrusive issues with the traditional approach versus these newer technologies. Thus, more elegant on-chip or onboard test techniques and circuits must be developed and validated [Mars05] that actually include the test signal generation and some of the capability to capture and/or partially reduce the raw test data.

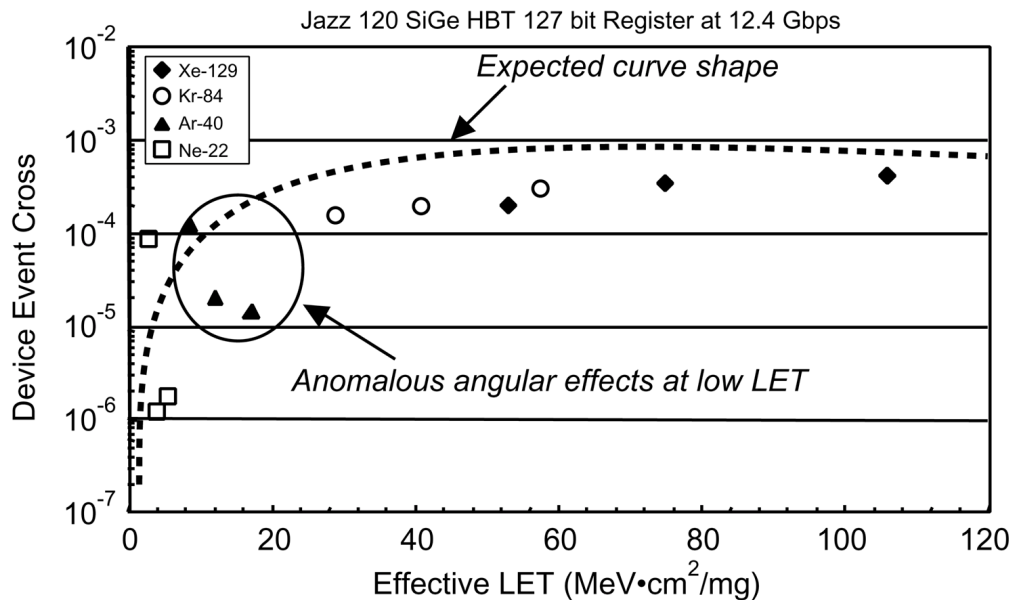
Figure 5: Effects of Protons in SOI



Effects of protons in SOI with varied angular direction of the particle;
Dashed line represents expected response with "standard" CMOS devices.

[Reed02]

Figure 6: Effects of Heavy Ions on SiGe Devices



Effects of heavy ions on SiGe devices at 12 GHz speeds notes anomalous charge collection of this high-speed technology;
 Drawn line represents expected response with "standard" models.

In general, test facility limitations are the result of the increasingly complex packaging systems that are being employed to support advanced IC's where > 1000 I/O pin counts are needed. The material systems and configuration of these packages provide a twofold deleterious effect concerning SEE testing and performance where; (1) the thickness of the package and inverted insertion of the chip greatly attenuate the beam LET making conservative testing impossible (except for at a few facilities) and, in addition, (2) the high Z materials generate secondary particles that contribute to the SER as a function of beam energy.

- **Modeling and Simulation Limitations:** As previously stated, the disparity of the results between modeled and measured SEE response [Well05] strongly suggests that our ability to model radiation effects in complex IC technology is severely limited. Specific areas of concern include the basic limitations and inaccuracies associated with existing transistor SPICE models, physics based Technology Computer Aided Design (TCAD) models and the compact radiation effects models derived from the test data and/or the more complex physics models.

5 Test Methods

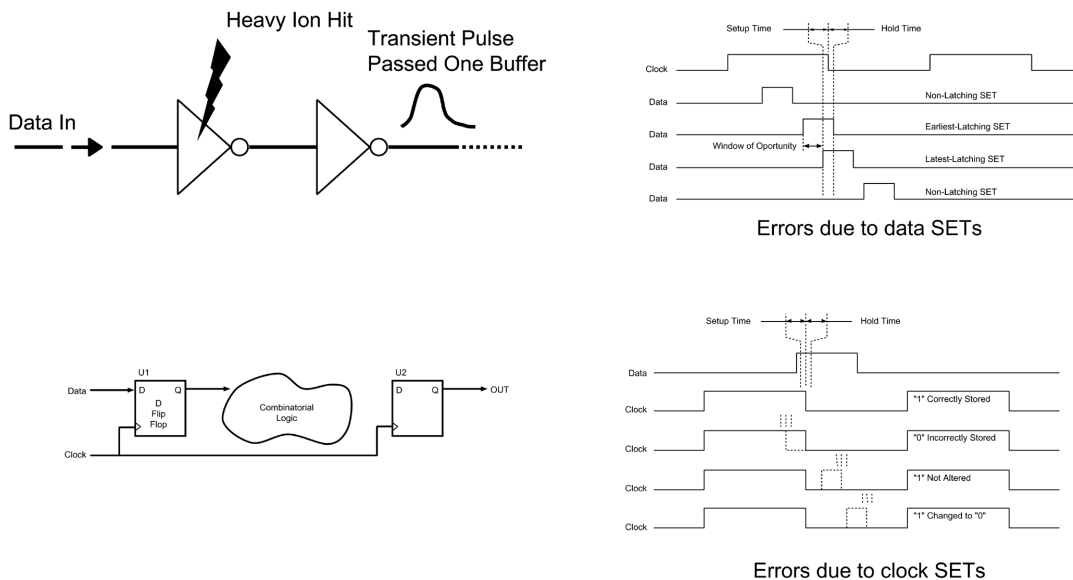
Next, with these issues in mind, we will examine present testing capabilities and techniques to identify specific shortfalls and issues.

5.1 SEE Testing:

In general, SEU testing, including MBU and SEFI characterization, is addressed by two test methods, JESD57 [JESD96] and ASTM 1192 [ASTM05], that focus on heavy ion testing. Additionally, a test method for Single Event Gate Rupture (SEGR) is also available in MIL-PRF-38535 [MIL02]. At present, there is not a specific method available that addresses SET.

Recall that an SET (also known as digital single event transient or DSET) is an upset caused by a voltage transient engendered in a combinational circuit that propagates to and is latched-in to a storage circuit such that it is mistaken for a real signal or data [Mavis02] as shown in **Figure 7**.

Figure 7: SET Errors in Sequential Circuits [Mavis02]



The bulk of the activity has been on SEU testing, however as circuit feature size keeps decreasing, circuit operating speed keeps increasing and suppliers continue to only address SEU hardening in sequential circuits, it is envisioned that SET effects will begin to dominate SEE error-rate response in the near future [Baum05]. Thus, it is imperative that SET error-rate prediction and test guidelines be generated in the near future.

The general approach to SEU characterization is well understood, however the issues engendered by circuit sensitivity that are a function of operation mode (e.g., a computation requiring intensive use of cache memory in a microprocessor versus another computation only requiring the Arithmetic Logic Unit (ALU)), operating speed, or other nuances of an IC's operation can be problematic WRT developing accurate error-rate predictions. In Figure 8, an example of a microprocessor's sensitivity as a function of operating mode is depicted [Howa01]. This issue can be exacerbated if an IC is comprised of different types of circuits (e.g. SRAM, ADC, Non-Volatile RAM (NVR), etc) with significantly different cross-sections and LET's. Such an example is shown in Figure 9 [Stur01].

Figure 8: Pentium III SEFI Heavy Ion Data [Howa01]

This is a sample of device operating mode SEE sensitivity.

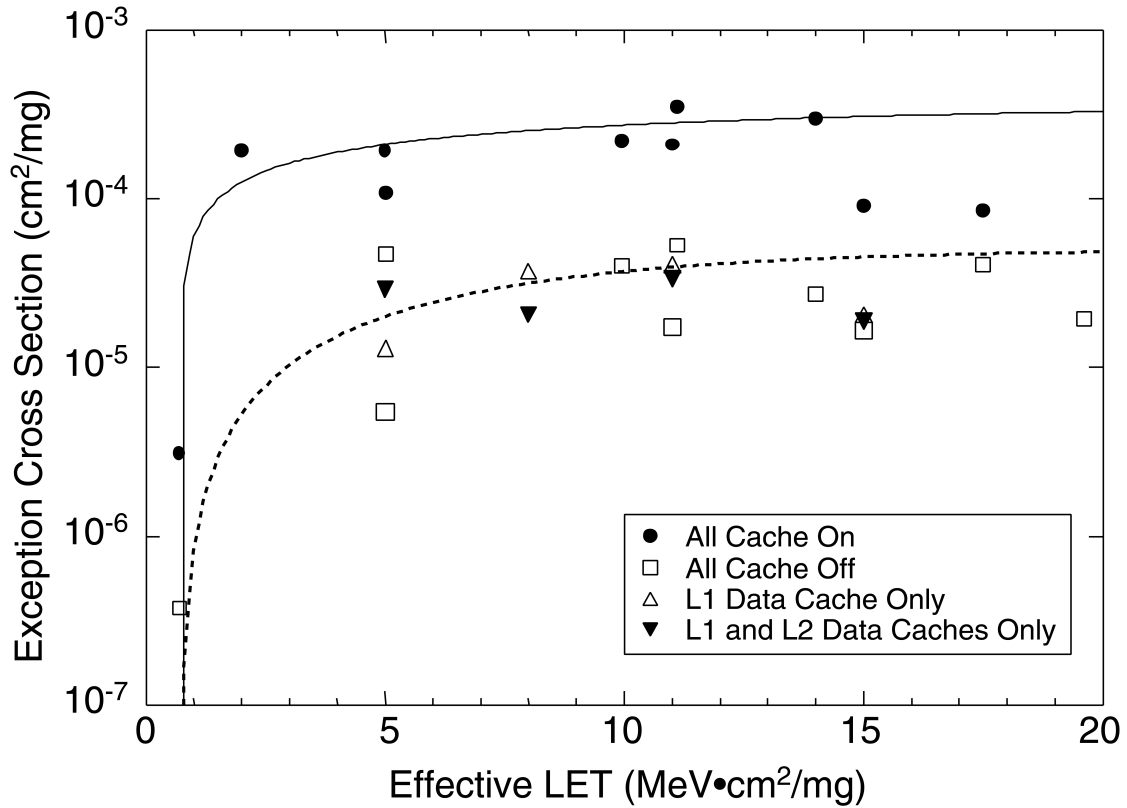
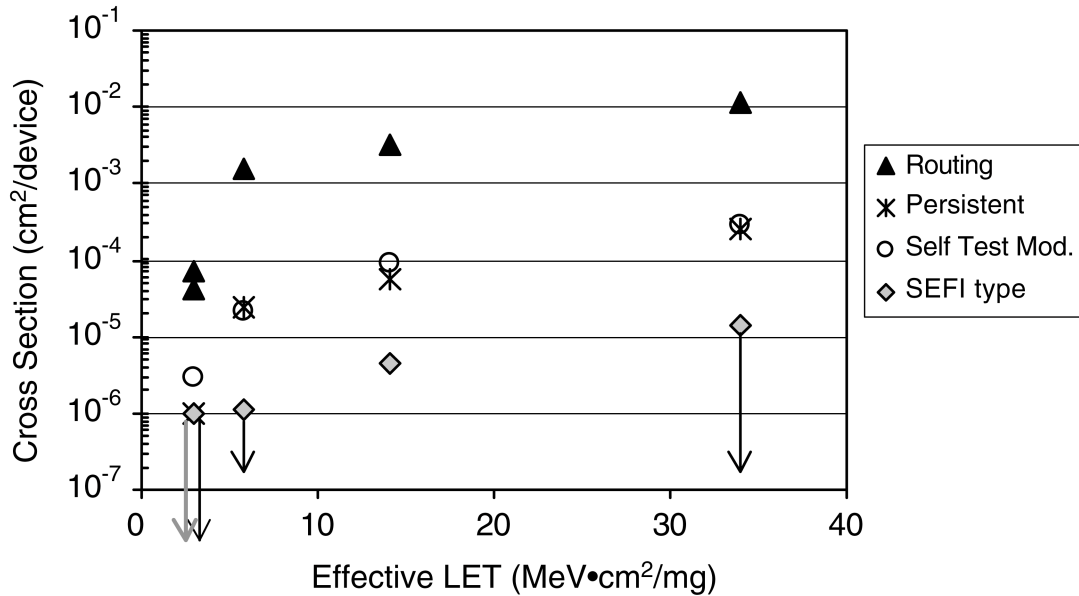


Figure 9: Configuration Errors in a latch-based (RAM) FPGA [Stur01]

The complexity of the circuit function provides many different error modes when a configuration bit is altered in these types of devices.



An assessment of the adequacy of SEU/MBU testing and characterization with respect to the advanced IC attributes and the relative impact of each attribute is summarized in Table 1 below. Note the effects of increasing intelligence, complexity and virtually all of the other attributes are to worsen SEU/MBU test and characterization.

Moreover, attributes such as construction, packaging and operating speed also influence decisions concerning the test facilities and diagnostics that can be used to perform the testing and characterization. Beam energy limitations at Brookhaven National Laboratory, for example, limit the type of circuit that can be tested making Texas A&M University (TAMU) and Berkeley National Laboratory the test facilities of choice. Indeed for some devices, depending on the packaging and device configuration, higher energy facilities such as the National Superconducting Cyclotron Laboratory (NSCL) at Michigan State University (MSU) and Ganil must be used. In Table 1, representative capabilities of various SEE test facilities generally available are shown for testing a packaged device assuming 1.5mm of plastic encapsulation.

Table 1: SEE Facility Energy/Range [Grimm00]

Facility	Ion (Energy)	LET Air - Plastic (MeV cm ² /mg)	LET Plastic - Si (MeV cm ² /mg)	Residual Range in Si
BNL	None*	NA	NA	NA
LBNL [#]	Neon (0.65 MeV)	1.4	4.8	75 μ m
LBNL [#]	Oxygen (0.52 MeV)	0.90	1.8	340 μ m
Texas A&M	None*	NA	NA	NA
MSU/NSCL [#]	Uranium (21 GeV)	46	80	320 μ m
MSU/NSCL [#]	Gold (21 GeV)	32	43	900 μ m

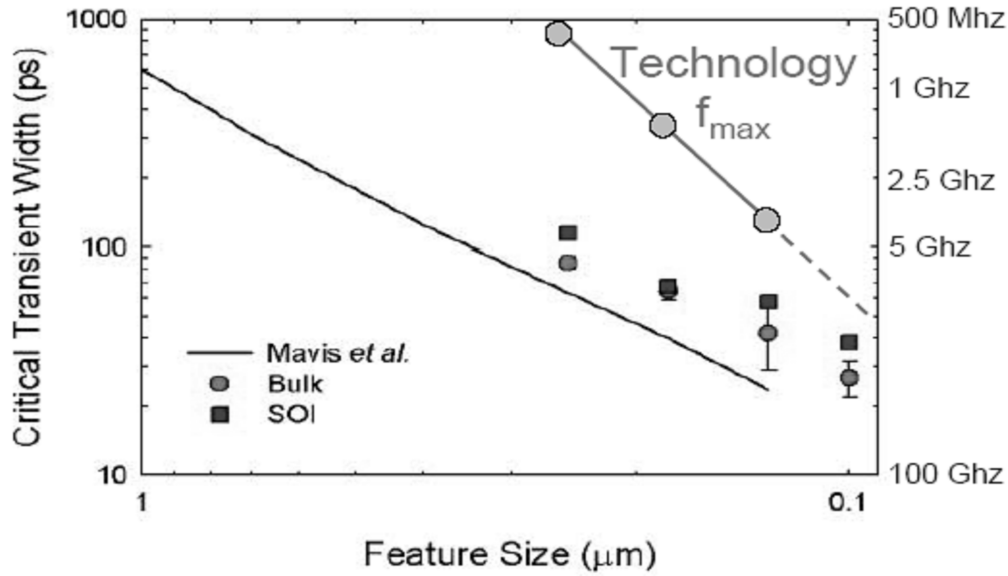
* None of the available ions with $Z > 1$ reach the Silicon die.

Other ions will reach the Si die, these examples are the ions that have the largest LET

5.2 SET Testing and Characterization:

SET testing and characterization represent a relatively new SEE issue. SET was predicted by Mavis [Mavis00] and others to become an issue as CMOS circuit feature size scaled below 0.25-microns. At that feature size it was predicted that the unattenuated propagation of voltage transients, caused by heavy ion strikes, would be sufficient to reach a storage (latch) type circuit in the vast majority of circuit designs. Indeed from Figure 10 that represents the results of modeling by both Dodd and Mavis, the propagation length of the transient is considered to be infinite.

Figure 10: SET Critical Pulse Width for Infinite Propagation



Adapted from P.E. Dodd, et al., "Production and Propagation of Single-Event Transients in High-Speed Digital Logic ICs," IEEE NSREC, 2004. [Dodd04-tns]

As seen in Figure 11, preliminary work by Marshall, et al [Mars04] showed an increase in IBM CMOS 5AM device sensitivity to heavy ion strikes as clock speed was increased to greater than 500 MHz with a major increase between the 400-600 MHz regimes. In particular, it is key to note that Marshall, et al have also demonstrated that single particle events can last longer than a single clock cycle (e.g., the pulse generated by a particle strike approaches 2 nanoseconds, thus when operating frequencies approach 500 MHz, multiple consecutive clock cycles can be corrupted). Further work by Benedetto, et-al [Bene04] has demonstrated the impact of operating frequency on SET error-rate and as can be seen from Figures 12 and 13, a three order of magnitude increase in error-rate can be realized for the DUT when going from 1 MHz to 300 MHz operation for both 0.18-micron and 0.25-micron test structures. Moreover, traditional SEU mitigation methods such as the dual-interlocked cell (DICE) latch are ineffective in mitigating this effect.

Figure 11: IBM 5AM SiGe Heterojunction Bipolar Transistor (HBT) DSET Data

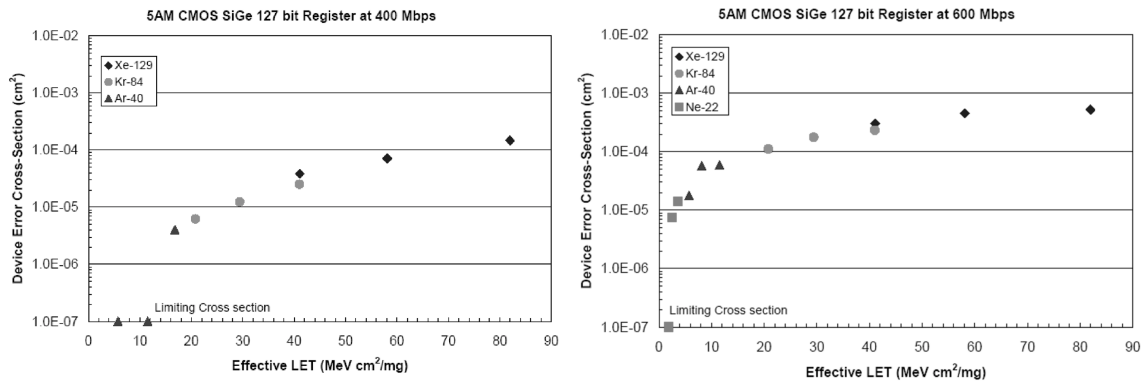


Figure 12: 0.18-micron DSET Data with Weibull Fits

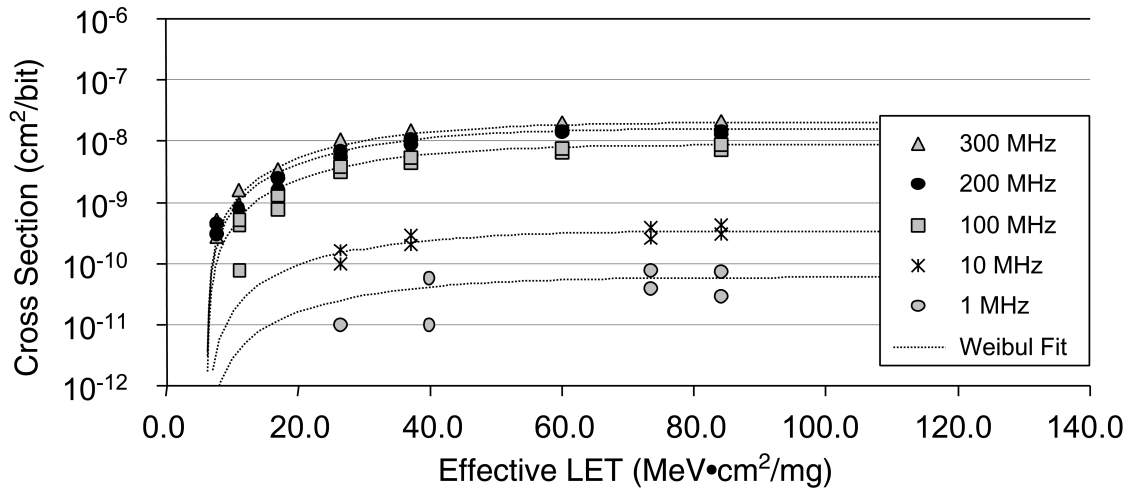
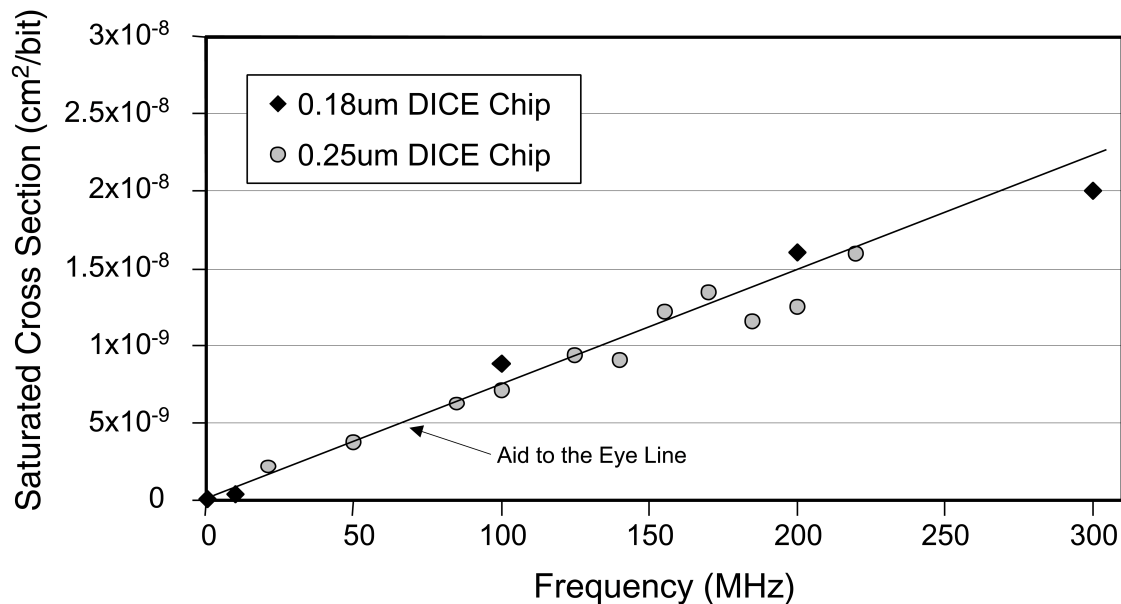


Figure 13: 0.18 and 0.25-micron DSET Error Cross Section versus Frequency



More recent testing of deep submicron technologies indicates that the SET effect may soon become the dominate factor in SEE error-rate generation, especially if circuits fabricated at these feature sizes are hardened against SEU effects.

As previously state there are no test methods or guidelines at present that specifically address SET and the present practice of SEE testing either precludes or makes it extremely difficult to perform testing at system operating speeds. Since testing at speed at present appears to be the only sure method of accurately determining SET error-rates, this represents a significant shortfall in our ability to characterize SER in complex IC's where the SER is comprised of both SEU and SET effects. As can be seen from Table 2, SET is exacerbated by most of the IC attributes associated with SEU.

The contrasts between SEU and SET are shown in Table 3. [Mavis00]

Table 2: IC Attribute Impact versus Radiation Test and Characterization

Attributes	SEU	MBU	SET	SEFI	SEGR	TID
Intelligence	++	++	+	++	-	-
Flexibility	++	++	-	+++	-	+
Complexity	+++	-	+	-	+	++
Integration Density	+	+++	-	-	-	-
Hidden Circuit Features	+	-	-	+++	-	-
Construction	++	++	++	++	++	++
Power	+	+	++	-	-	-
Speed	-	-	+++	-	-	-

+ = worse

++ = much worse

+++ = very significant impact

- = no effect

Table 3: Comparison of SEU versus SET Mavis, 2001 [Mavis00]

- Conventional Static Latch Upset (SEU)
 - Junction collection in static latches & SRAMs
 - Voltage transient magnified by circuit feedback
 - Data state of latch flips if switch point crossed
 - Critical charge decreases as (FS)²
- Single-Event-Transients (SET)
 - Junction collection in combinational circuits
 - Voltage transient no longer attenuated in submicron devices
 - Incorrect data latched in at clock edge
 - Critical width for unattenuated propagation decreases as (FS)²
 - Error rates increase in proportion to clock frequency

5.3 SEFI:

The issues associated with SEFI in complex IC's has been studied for a number of years. Researchers from GSFC, for example, noted this effect in DRAM technology [LaBel96]. SEFI for this discussion also includes "hang" type responses in microprocessors [Swift01] and SRAM based FPGA loss-of-configuration fail modes [Katz98], [Hoff00]. The primary issue with most SEFI events is that the root cause cannot be determined since the critical circuits (registers, logic control, etc.) involved are often not identified by the manufacturer (Hidden Circuit Feature Attribute). Moreover, the ability to reverse engineer these complex IC's to identify root cause problems is prohibitively difficult.

Testing and characterization is a problem since a SEFI event may be operating mode and duty cycle sensitive and only happen when certain interactions between a cache memory and a set of specific registers is occurring. This, of course, places stringent requirements on radiation testing concerning the selection of the DUT operating mode during testing, the selection of the input vectors, and device coverage.

At present there are no guidelines or specific test methods that address SEFI testing and characterization.

5.4 SEGR:

Although SEGR is an issue that has been generally discussed in conjunction with power high voltage semiconductor devices, it is also relevant to advanced microelectronics. Specifically, as gate oxide thicknesses continue to follow the scaling rules, the potential for a rupture caused by the strike of a single energetic particle becomes more likely. Testing, to-date by Massengill and Sexton, et-al, [Mass01-tns], [Wrob87], [Fish87], [Lum04], [Sext98], [Sext97], [John98], [Mons02] has not indicated the existence of an immediate problem, however this is an issue that must remain on our watch-list. Moreover, there is no one test method or guideline that addresses SEGR for low power electronics. A more cogent issue concerning SEGR has to do with the use of drop-in non-volatile memory that uses higher than normal operating voltage to implement erase and write functions in large application specific IC (ASIC) or System on Chip (SOC) devices. For this situation, a particle strike during the application of the high voltage has the potential to engender a SEGR event. Moreover, as previously identified for low voltage logic type devices, there is no test method or guideline to support users. In addition, no body of knowledge is available at this time concerning this failure mode for drop-in non-volatile memory for deep submicron technology.

5.5 TID:

Recent testing [Lacoe03] has shown that the impact of scaling has served to improve steady state TID performance for low voltage CMOS and heterojunction bipolar transistor (HBT) technologies. The combination of very thin gate oxides and shallow trench isolation has made it possible to achieve satisfactory TID performance at levels as high as 300 krad(Si).

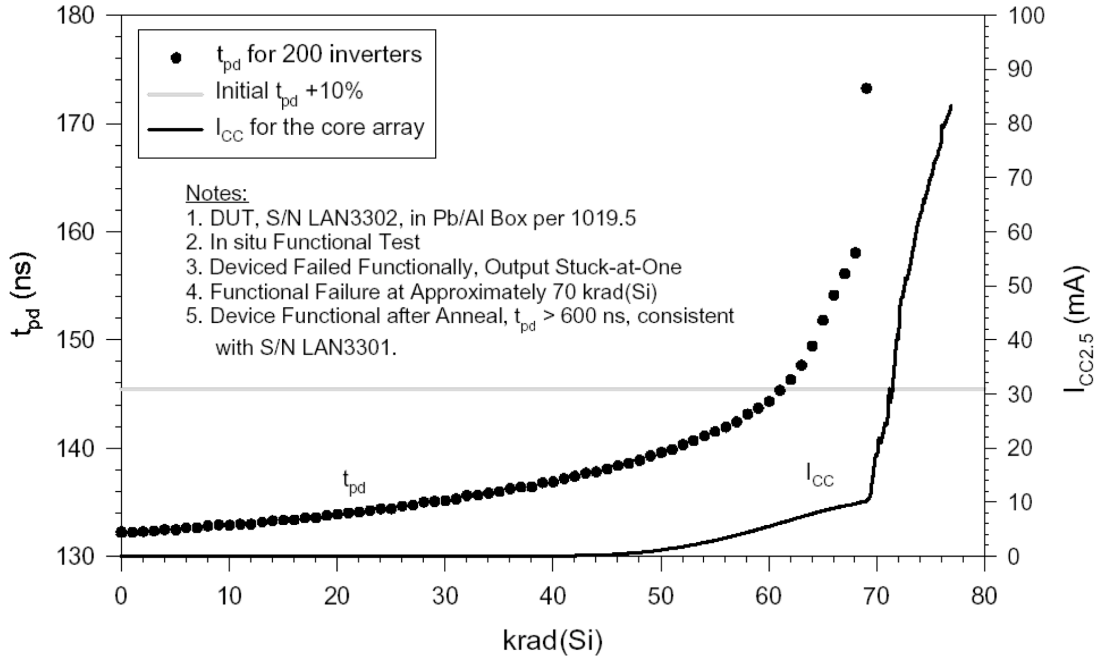
However, several areas still of concern include:

- Embedded electrically erasable programmable read-only memory (EEPROM) programmable drop-ins wherein TID will impact the charge stored on the EEPROM floating gate and has the potential to effect the circuit configuration.
- Embedded programmable drop-ins or other circuits that use charge-pump circuits to develop higher than applied operating voltage potentials to ensure the proper operation of pass-gate devices as shown in Figure 15. [klabs02]

Thus, despite the generally improved performance, a TID evaluation of advanced ASIC and SOC devices is required to ensure that "sensitive" sub-circuits are not embedded on the overall low voltage CMOS design.

Additionally, several test method and guideline documents exist to support this type of characterization, for example MIL-STD-883 1019.6. [MIL-STD]

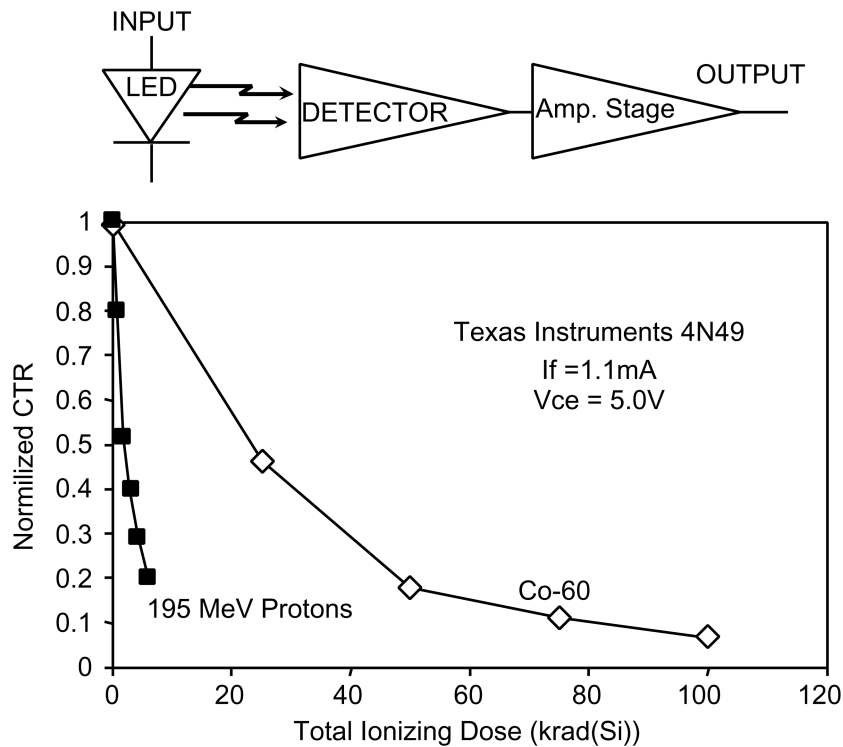
Figure 15: The impact of total ionizing dose irradiation of the operation of a one-time programmable FPGA utilizing a charge pump circuit



5.6 Displacement Damage Testing and Characterization:

Displacement damage effects have generally not been an issue with either the CMOS or HBT technologies that we can anticipate being used for advanced microelectronics applications. However, with the growing use of embedded optoelectronics [MIT05] to facilitate isolation and data transfer applications, the need to perform displacement damage testing should be recognized. In a graphic example, Rax, et-al [Rax96] demonstrated the danger of neglecting this aspect of flight qualification testing for an opto-isolator as shown in Figure 16.

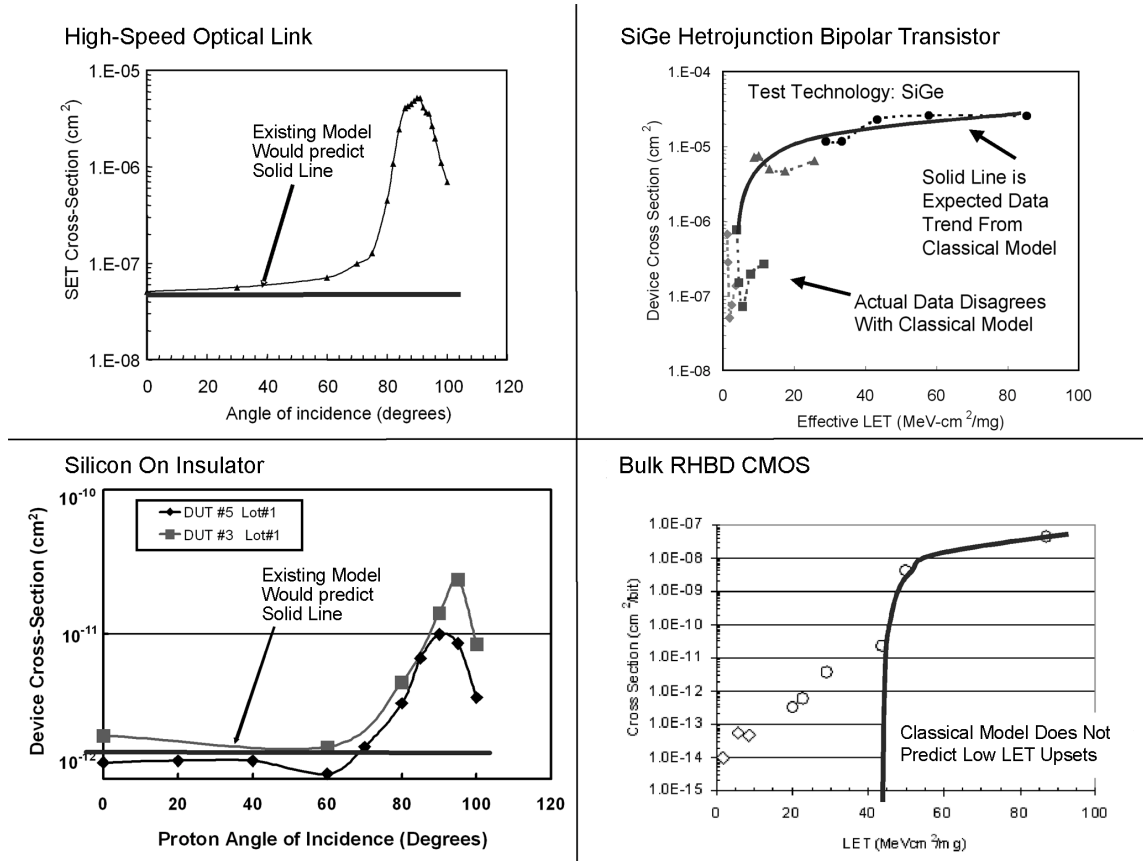
Figure 16: The effects of Co-60 (gamma) versus proton irradiation on an Opto-Coupler Device high-lighting the effects of displacement damage on Current-Transfer-Ratio (CTR)



5.7 Modeling and Simulation Issues

Radiation response modeling and simulation support for deep submicron technology represents one of the areas where major shortfalls exist. This is a pervasive issue that includes Electronics Design Automation (EDA), TCAD, mixed-mode modeling and models that provide an accurate representation of the interaction of energetic particles with deep submicron semiconductor devices including metal over-layer secondary production effects [Well04]. Some of the issues with respect to modeling and simulation (M&S) shortfalls are shown in Figure 17.

Figure 17: Modeling and Simulation Shortfalls



6 Mitigation Methods

A rich body of knowledge exists concerning SEE mitigation and the associated performance, power and area penalties for the various methods. In this section, we will examine each of the failure modes described in Sections 3 and 4 and provide a discussion concerning the mitigation methods now in place, their limitations and associated penalties.

6.1 SEU and MBU:

SEU/MBU mitigation represents the most widely studied area and vast amounts of effort have gone into the mitigation of this effect. The approaches can be roughly divided into two areas that are:

- Process and materials related approaches
- Circuit design and layout related approaches

Additionally, it should be noted that the approaches are often used in layers or combined in various ways.

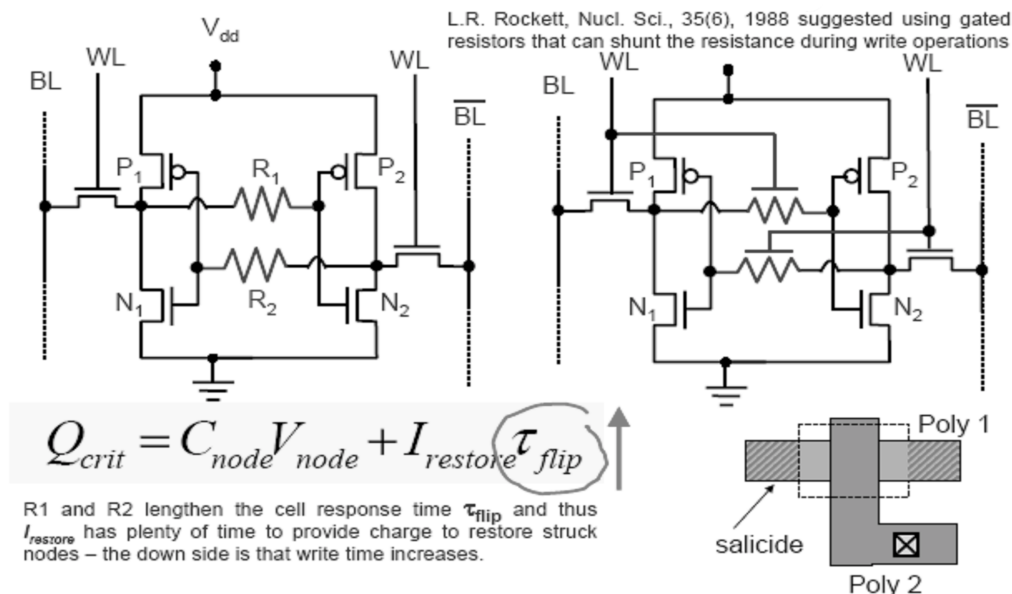
6.1.1 Process and Layout Approaches:

Concerning process related approaches, the one most commonly used is the insertion of an resistor-capacitor (RC) network into the feedback path for a latch circuit as shown in Figure 18.

While this method has been effective in the past there are a number of drawbacks to this approach that include:

- The adverse impact on memory cell write time caused by the RC delay. Note that the use of an electrically gated resistor approach can ameliorate this shortcoming at the cost of increased circuit complexity. Also, the loss of SEU protection during the write cycle can be construed as a shortfall.
- The issues involved with the use of an RC network include increased process complexity due to the need for a low doped poly-silicon resistor module in the process flow. In addition, the positive temperature coefficient associated with the resistor results in a change in SEU immunity across operational temperature range.
- The need too insert a “large “ capacitor in the cell can also impact reliability due to issues with oxide integrity, however this has not proved to be a major problem.
- Cell design issues concerning density resulting from the insertion of the RC network. N.B. - Contemporary approaches have partially resolved this problem by inserting the RC network above the memory cell.

Figure 18: Resistive Hardening SEE Hardening for a Memory Cell



Concerning submicron technologies that can upset at very low charge values, the very large resistor value (e.g., > 1Mohms), required to reduce SER to an acceptable value, have made the direct use of this technique difficult since there is a finite limit to the ohms-per-square that can be obtained. A method that has been used to extend this approach has been to use it in conjunction with an insulating substrate (e.g., SOI) to reduce charge collection and hence reduce the required resistor size.

Other processing approaches include the use of low resistance epitaxial layers on bulk (or SOI) substrates and/or an insulating substrate to reduce the charge collection volume. It has been shown that the use of an SOI substrate provides an order of magnitude decrease in error rate can be achieved over comparable bulk silicon technology.

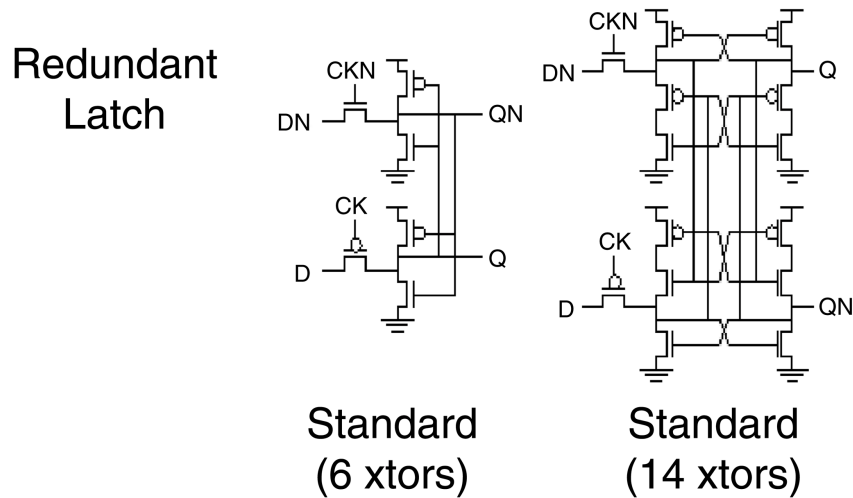
Another processing approach that is also used to achieve improved electrical performance has to do with the use of a retrograde well design where the doping density increases with well depth. The higher doped lower layer serves in much the same way as the above noted epitaxial layer to cut-off the charge track and reduces the collected charge.

Finally, it has been proposed that the use of the retrograde approach be extended to insert a highly doped buried layer to provide a sink for the deposited charge.

6.1.2 Circuit Design and Layout Approaches:

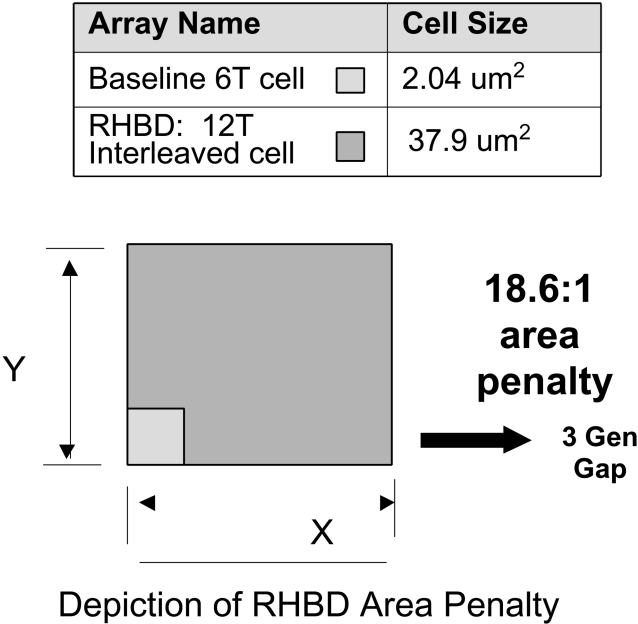
At the circuit design level, a number of approaches exist that are all related to the insertion of added transistors in traditional latch designs to preclude cell upset. A number of the design approaches are shown in Figure 19 and include 10 and 14 transistor memory cells and other such configurations [Boeing05].

Figure 19: Circuit Design Approaches



The benefits of a design approach in general relate to their ability to be assimilated into almost any fabrication process and be supported by standard design libraries. However, the related area and power penalties associated with this approach are significant as demonstrated in Figure 20 that compares a 12T memory cell with a 6T cell [Boeing05]. Thus, while effective in suppressing SEU this approach does not necessarily lend itself to the fabrication of high-density memory devices.

Figure 20: Rad-Hard by Process (RHBP) versus Pure Rad-Hard by Design (RHBD) Performance Comparison; DARPA RHBD Program, March 2005



Other less obvious problems with the above noted approaches include the fact that upset is not precluded if multiple nodes are struck and the designs do not address SET mitigation.

Two layout approaches that are often used concurrently with these design approaches include the use of word bit physical location staggering and critical node interleaving. The placement of bits within the same word in physical locations that preclude being struck by a single ion is an approach that supports error detection & correction (EDAC) by limiting the corrections to single vice multiple bits and thus simplifying correction and detection circuit design. Critical node inter-leaving refers to the layout practice of placing nodes within a cell in locations that preclude or at least significantly reduce the probability of a multiple node strike that can obviate the effectiveness of these design approaches as shown in Figure 21.

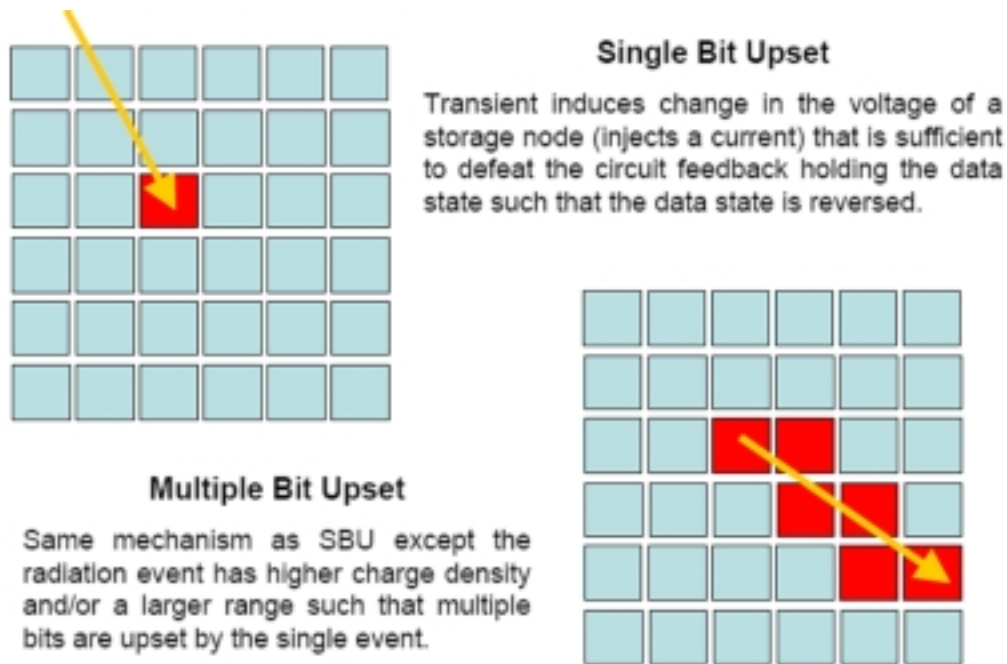
At a higher level of integration density, techniques that include, but are not limited to, error-correction and detection and voting through triple or more modular redundancy can be employed. EDAC methods come in many shapes and sizes and include a variety of algorithms such as the Hamming Code, Reed-Solomon, etc., but each of these must be evaluated versus word length, latency, circuit complexity, area, power, etc. [Heid99].

The negative impacts of EDAC and voting can be summarized as:

- Additional circuitry that impacts power and density
- The need to periodically scrub the protection circuits to eliminate latent errors that result in increased system design complexity.
- Reductions in system throughput due to the increased circuit levels needed to implement these methods.

In closing, there are a number of techniques that can be applied to mitigate SEU/MBU and, depending on system availability requirements, these approaches can be applied in a layered manner to achieve operating goals.

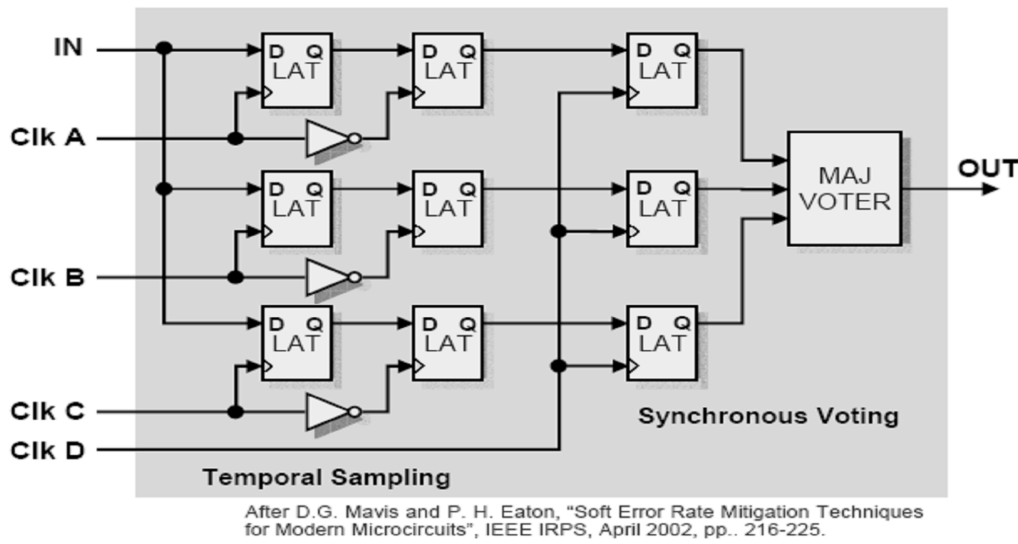
Figure 21: SEU versus MBU [Baum05]



6.2 SET:

At present, the basic approach to mitigate SET involves the use of a circuit denoted as the Temporal Latch, as shown in Figure 22 [Baum05] that in essence is a triple module redundant (TMR) circuit aligned to compare voltage transients that can be separated as a function of pulse width. Specifically, the method depends on a fairly precise knowledge of the transient pulse width and the ability to operate the circuit (or system) at speeds that allow one to use a pulse width that is $\sim 2X$ the transient pulse width. Thus, if a transient pulse created from an ion strike is measured for a technology to be 1ns, the maximum operating speed of the system would be limited to 500 MHz. Obviously such a limitation could impose onerous restrictions on system operation. SET effects have not been analyzed to the extent of SEU since it has only become a problem as feature size has been scaled to < 0.25 -microns. Above this feature size, the transient induced pulse widths were insufficiently wide to allow for significant stage-to-stage propagation and thus were not evident. However, as was seen from Figures 12 and 13 [Mavis02], this is no longer the case.

Figure 22: SET & SEU Hardened Latch (Temporal Latch)



In addition to the circuit design mitigation approach, any or all of the processing approaches that reduce charge collection volume would be appropriate to reduce the amplitude and width of the voltage transient caused by the energetic particle strike.

6.3 SEFI:

In principle, all of the techniques available to mitigate SEU effects are appropriate for SEFI, with the exception of EDAC and thus, SEFI mitigation should be a generally straight-forward issue. However, this is seldom the case, since a SEFI response is usually the result of some unidentified part of a complex circuit being upset and the user has little or no insight into the root cause of the response. Moreover, obtaining this level of information from the manufacturer is not viable. Additionally, for complex microprocessors, the SEFI or “Hang” response can be a function of the immediate operation of the circuit (e.g. interaction between the application program, specific computation and cache memory), making the mitigation of the SEFI all but impossible. SRAM based reconfigurable FPGA devices can also fall victim to a SEFI that inadvertently reconfigures the programmed architecture.

Concerning SEFI mitigation for standard IC’s, system level approaches such “Watch-Dog” timers, frequent critical circuit configuration bit comparisons, scrubbing and other external approaches can be used.

However, as previously noted, these external monitoring and control circuits must be radiation hardened and add to system overhead.

6.4 SEL:

The mitigation of SEL can also be delineated into (1) a process and materials approach and a (2) design and layout approach.

Concerning processing and material, the use of an insulating substrate or an epitaxial layer to impact the parasitic bipolar transistor’s operation have been used effectively in the past. The insulating layer eliminates the formation of the silicon-controlled rectifier (SCR) circuit. The low resistance epitaxial layer prevents the SCR from turning on by shunting the base resistor with a low impedance path for the charge and thus the SCR never goes into forward bias and Latchup.

Concerning design and layout, the use of a guard ring around each CMOS device interrupts the SCR structure, precluding turn-on. Additionally, by increasing well spacing, the combined gain of the parasitic transistors can be reduced to eliminate latchup.

Approaches to SEL circumvention has been widely discussed and can be found in [Kinn98] [Trout86] [Estr80] [Dawes76]

The impact of these mitigation methods either involves an increase in process complexity or some area penalty to insert either a guard ring to separate the n-channel and p-channel transistors.

7 Recommendations:

Thus, based on the discussion of Section 5.0, a number of recommendations concerning areas that require additional support are provided as follows:

- Improved understanding of extreme value statistics as it applies to radiation particle impacts
- Development of High-Energy SEU Micro-beam [Lad04] and TPA Laser [McMo04]
- Development and validation of System Risk Tools
- Development of Portable High-Speed Device Testers
- Development of a Physics Based Modeling Tool and an efficient mixed-signal modeling capability [Well04]
- Development of substrate engineering processing methods to decrease charge generation and enhance recombination.

While it is not suggested that the availability of these methods will provide a panacea concerning the resolution of the issues identified in Section 5.0, it is envisioned that they will provide a foundation to support the use of advanced deep submicron microelectronics for high reliability space applications.

8 Summary and Conclusions

Concerning the areas of testing, modeling and simulation, a number of shortfalls and/or deficiencies with our present capabilities can be identified. These would include the absence of dedicated test methods and guideline documents as well as limitations concerning modeling and simulation of both SEE and TID in these ultra-deep submicron technologies. These issues have been discussed in some detail in the preceding sections and are summarized in the Table 4, below.

Table 4: Summary of testing and modeling and simulation support for Advanced Microelectronics

Radiation Response	Guideline Document	Test Method	Data Base	Modeling & Simulation
SEU/MBU	Yes	Yes	Yes	~ mature
SET	No	No	No	No
SEL	Yes	Yes	Yes	No
SEGR	No	No	No	No
SEFI	No	No	No	No
TID	Yes	Yes	Yes	Yes
Displacement Damage	Yes	Yes	No	No

As can be seen and inferred from the number of areas that are shaded red there are significant shortfalls concerning our ability to support testing and model and simulate the most of the effects of radiation induce degradation of these technologies. Moreover, in many cases, there is a lack of test data to support space applications.

In addition, an examination of the presently available and well understood mitigation methods reveals that the majority involve penalties in both area and power that significantly erode the performance and integration density improvements afforded through the use of advanced microelectronics technologies.

Moreover, from the discussion of Section 5.0 on modeling and simulation, we note that there are also profound issues concerning the present fidelity of our simulation capabilities.

9 References:

- [radhome] NASA/GSFC Radiation Effects and Analysis home page,
<http://radhome.gsfc.nasa.gov>
- [ITRS01]. International Technology Roadmap for Semiconductors web site
<http://public.itrs.net/>
- [Dell05] Arlene Dellin and Theodore Dellin, 21st Century Semiconductor Technology Handbook, Quick Start Micro Training LLC, <http://www.quickstartmicro.com/handbook.htm>, 2005.
- [Mass01-Van] Adapted from Lloyd W. Massengill, Single Event Circuit Effects, Vanderbilt Radiation Effects Course, <http://www.mrchsv.com/docs/Vanderbilt/Transient-SEE%20-%20Lecture.pdf>, Aug. 2001.
- [Bene04] J. Benedetto, et al., "Heavy Ion-Induced Digital Single-Event Transients in Deep Submicron Processes," IEEE Trans. Nucl. Sci., Vol. 41, No. 6, pp 3480-3485, Dec. 2004.
- [Hadd05] Haddad, private communication, June 2005.
- [Irom04] F. Irom and F.F. Farmanesh, "Frequency dependence of Single-Event Upset in Advanced Commercial PowerPC Microprocessors," IEEE Trans. Nucl. Sci., Vol. 41, No. 6, pp 3505-3509, Dec. 2004.
- [Bose05] G. Boselli, V. Vijay and C. Duvvury, "Latchup in 65nm Technology: A Scaling Perspective" 43rd IEEE International Reliability Physics Symposium Proceedings, pp 137-144, 2005.
- [Chat04] K Chatty, P. Cottrell, R Gauthier, M. Muhammad, F. Stellari, A. Wegner, P Song, and M McManus, "Model-Based Guidelines to Suppress Cable Discharge, Event (CDE) Induced Latchup", 42nd IEEE International Reliability Physics Symposium Proceedings, pp 130- 134, 2004.
- [Salc03] J. Salcedo-Suner, R. Cline, C. Duvvury, A. Cadena-Hernandez, L. Ting, and J. Schichl, "A New IO Signal Latchup Phenomenon in Voltage tolerant ESD Protection Circuits", 41rd IEEE International Reliability Physics Symposium Proceedings, pp 85-91, 2003.
- [Dodd04-IRPS] P.E. Dodd, M.R. Shaneyfelt, J.R.Schwank, and G. Hash, "Neutron-Induced-Latchup in SRAMs at Ground Level", 42rd IEEE International Reliability Physics Symposium Proceedings, pp 51- 55, 2004.
- [Swift05] G. Swift, et al., "Preparation of Devices for Single Event Testing," DRAFT JPL NASA document, 2005.
- [Mars05] P. Marshall, et al., "Autonomous Bit Error Rate Testing at multi-Gbit/s Rates Using a Circuit for Radiation Effects Self Test (CREST)," submitted to IEEE Trans. Nucl. Sci., Dec. 2005.
- [Reed02] Robert A. Reed, et al., "Evidence for Angular Effects in Proton-Induced Single-Event Upsets," IEEE Trans. Nucl. Sci., Vol. 49, No. 6, pp 3038-3044, Dec. 2002.
- [Well05] Weller, et al (Vanderbilt), "Modeling Semiconductor Device Response Using Detailed Radiation Event Simulations," presented at Hardened Electronics and Radiation Technology (HEART) Meeting, Mar 2004.
- [JESD96] "Test Procedure for the Management of Single-Event Effects in Semiconductor Devices from Heavy Ion Irradiation," JC-13.4 Subcommittee, <http://www.jedec.org/Catalog/display.cfm>, JESD 57, Dec. 1996.
- [ASTM05] "F1192-00 Standard Guide for the Measurement of Single Event Phenomena (SEP) Induced by Heavy Ion Irradiation of Semiconductor Devices," Book of Standards Volume 10.04, ASTM International, Developed by Subcommittee, <http://www.astm.org>, F1192-00, 2005.

- [MIL02] "Performance Specification, Integrated Circuits (Microcircuits) Manufacturing, General Specification For," Department of Defense pub MIL-PRF-38535F, <http://www.dscc.dla.mil/Downloads/MilSpec/Docs/MIL-PRF-38535/prf38535.pdf>, Dec. 2002.
- [Mavis02] D.G. Mavis and P.H. Eaton, "Soft Error Rate Mitigation Techniques for Modern Microcircuits," IEEE IRPS, pp 216-225, April 2002.
- [Baum05] Robert Baumann (Texas Instruments), "Single-Event Effects in Advanced CMOS Technology," IEEE NSREC Short Course, Short Course, Sect. II, pp 1-59, July 2005.
- [Howa01] James W. Howard, Jr., et al., "Total Dose and Single Event Effects Testing of the Intel Pentium III (P3) and AMD K7 Microprocessors," IEEE Radiation Effects Data Workshop, pp 38-47, July 2001.
- [Stur01] F. Stureson, et al., "Radiation Pre-Evaluation of Xilinx FPGA XQVR300", European Space Agency Contract Report, Doc. No. D-P-REP-1091-SE, Aug 2001.
- [Grimm00] T. Grimm (MSU), "Construction of a Single Event Effects Test Facility at the NSCL," SEESYM Apr. 2000. Also available at High Energy Heavy Ion Single Event Effects (SEE) Test Facility at the National Superconducting Cyclotron Laboratory (NSCL) at Michigan State University (MSU) http://radhome.gsfc.nasa.gov/radhome/papers/NSCL_May00_files/frame.htm
- [Mavis00] D.G. Mavis, and P. H. Eaton, "SEU and SET Mitigation Techniques for FPGA Circuit and Configuration Bit Storage Design," MAPLD, Sept. 2000.
- [Dodd04-tns] P.E. Dodd, et al., "Production and Propagation of Single-Event Transients in High-Speed Digital Logic ICs," IEEE Trans. Nucl. Sci., Vol. 41, No. 6, pp 3278-3284, Dec. 2004.
- [Mars04] P. Marshall, et al., "A Comparative Study of Heavy-Ion and Proton-Induced Bit-Error Sensitivity and Complex Burst-Error Modes in Commercially Available High-Speed SiGe BiCMOS," presented at SEESYM, April 2004.
- [LaBel96] K. LaBel, et al., "Radiation Effects Characterization and Test Methods of Single-Chip and Multi-Chip Stacked 16 Mbit DRAMs," IEEE Trans. Nucl. Sci., Vol. 43, No. 6, pp 2974, Dec. 1996.
- [Swift01] G.M. Swift, et al., "Single-event upset in the PowerPC750 microprocessor," IEEE Trans. Nucl. Sci., Vol. 48, No. 6, Pt. 1, pp1822-1827, Dec. 2001.
- [Katz98] R. Katz, et al., "Current radiation issues for programmable elements and devices," IEEE Trans. Nucl. Sci., Vol. 45, No. 6, Pt. 1, pp 2600-2609, Dec. 1998.
- [Hoff00] L. Hoffman, et al., Radiation Effects Testing of Programmable Logic Devices, IEEE NSREC Short Course, Sect. V, pp 1-65, July 2000.
- [Mass01-tns] L. Massengill, et-al, "Heavy-ion-induced breakdown in ultra-thin gate oxides and high-k dielectrics," IEEE Trans. Nucl. Sci., Vol. 48, No. 6, pp 1904-1912, Dec. 2001.
- [Wrob87] T.F Wrobel, "On Heavy Ion Induced Hard-Errors in Dielectric Structures," IEEE Trans. Nucl. Sci., Vol. 34, pp1262-1268, Dec. 1987
- [Fish87] T. A. Fisher, "Heavy-Ion-Induced, Gate-Rupture in Power MOSFETs," IEEE-Trans. Nucl. Sci., Vol. 34, pp 1786-1791, Dec. 1987.
- [Lum04] G. Lum, et-al, "New experimental findings for single-event gate rupture in MOS capacitors and linear devices," IEEE Trans. Nucl. Sci., Vol. 51, pp 3263-3269, Dec. 2004.
- [Sext98] F Sexton, et-al, "Precursor ion damage and angular dependence of single event gate rupture in thin oxides," IEEE Trans. Nucl. Sci., Vol. 45, pp 2509-2518, Dec. 1998.

- [Sext97] F Sexton, et-al, "Single event gate rupture in thin gate oxides," IEEE Trans. Nucl. Sci., Vol. 44, pp 2345-2352, Dec. 1997.
- [John98] A.H. Johnston, "Breakdown of gate oxides during irradiation with heavy ions," IEEE Trans. Nucl. Sci., Vol. 45, No.6, pp 2500-2508, 1998.
- [Mons02] F Monsieur, et-al, "A Thorough Investigation of Progressive Breakdown in Ultrathin Oxides, Physical Understanding and Application for Industrial Reliability Assessment," in Proc. IRPS, pp 45-54, 2002.
- [Lacoe03] R. Lacoe, "CMOS Scaling, Design Principles and Hardening-By-Design Methodologies," IEEE NSREC 2003 Short Course, Sect. II, pp 1-142, July 2003.
- [klabs02] http://klabs.org/richcontent/fpga_content/ProASIC/LAN3300/k050.pdf.
- [MIL-STD] Department of Defense Test Method Microcircuits, MIL-STD-883 Test Method Standard, Microcircuits, MIL-STD-883 Test Method 1019.6, Dated: 07 March 2003, File name: std883not5.pdf, <http://www.dscc.dla.mil/Downloads/MilSpec/Docs/MIL-STD-883/std883not5.pdf>
- [MIT05] MIT Technology Review Magazine, "Emerging Technologies – Silicon Photonics," http://www.technologyreview.com/articles/05/05/issue/feature_emerging.asp?p=3, May 2005.
- [Rax96] Rax, et al., "Total dose and proton damage in optocouplers," IEEE Trans. Nucl. Sci., Vol. 43, No. 6, pp 3167-3173, Dec. 1996.
- [Well04] Weller, et al (Vanderbilt), "Modeling Semiconductor Device Response Using Detailed Radiation Event Simulations," presented at Hardened Electronics and Radiation Technology (HEART) Meeting, Mar 2004
- [Boeing05]. Boeing review for DARPA Rad-Hard by Design Program, Mar. 2005.
- [Heid99] W.F. Heidergott (Motorola Inc.), "System Level Mitigation Strategies," IEEE NSREC Short Course, Sect V, pp 1-68, July 1999.
- [Kinn98] J.D. Kinnison, "Achieving Reliable, Affordable Systems," IEEE NSREC Short Course, Sect. V, pp 1-41, July 1998.
- [Trout86] T. Troutman, "Latch-up in CMOS Technology," Kluwer Academic Publisher, 1986.
- [Estr80] D. Estreich, "The Physics and Modeling of Latch-up in CMOS Integrated Circuits," Tech. Report Number G-201-9, Standord Electronics Lab., Stanford University, 1980. Trans. Nucl. Sci., Vol. 23, pp 2027-2030, Dec. 1976.
- [Dawes76] W. Dawes, Jr. and G. Gerbenwick, "Prevention of CMOS Latch-up in MOS Integrated Circuits," IEEE
- [Lad04] Ray Ladbury, "The Inaugural SEE Run for the NSCL SEE Test Facility," SEESYM, A4, April 2004.
- [McMo04] D. McMorow, et al., "Demonstration of single-event effects induced by through-wafer two-photon absorption," IEEE Trans. Nucl. Sci., Vol. 54, No. 6, pp 3553-3557, Dec 2004.